Listing of Claims

1. (currently amended) A system for processing applications, the system comprising:

a plurality of processor nodes with each processor node comprising:

a processing element configured to execute at least one of the applications~~,~~;

a software extensible device configured to provide additional new instructions to a set of standard instructions for the processing element, wherein the new instructions can be programmed by software~~,~~;

a first communication interface including a first array interface module configured to interface to a first other member of the plurality of processor nodes, and a first standard input/output interface configured to communicate with a first input/output device,

a second communication interface including a second array interface module configured to interface to a second other member of the plurality of processor nodes, and a second standard input/output interface configured to communicate with a second input/output device; and

~~a communication interface configured to communicate with other processor nodes using different communication protocols based on whether or not a neighboring processor node comprises another~~

~~software extensible device and whether the neighboring processor node is on a separate chip or on a same chip; and~~

a plurality of links interconnecting the plurality of processor nodes.

2. (previously presented) The system of claim 1 wherein each one of the processor nodes are on separate chips.

3. (original) The system of claim 1 wherein at least some of the processor nodes are on the same chip.

4. (currently amended) The system of claim 1 wherein two or more of the plurality of the processor nodes are configured in an array.

5. (original) The system of claim 1 wherein the software extensible device comprises an instruction set extension fabric.

6. (original) The system of claim 1 wherein the software extensible device comprises a programmable logic device.

7. (canceled)

8. (currently amended) The system of claim 1 wherein at least one of the first communication interface and the second ~~the~~ communication interface is configured to communicate using message passing.

9. (currently amended) The system of claim 1 wherein at least one of the first communication interface and the second ~~the~~ communication interface is configured to communicate using channels between the processor nodes.

10. (currently amended) The system of claim 9 wherein at least one of the first communication interface and the second ~~the~~ communication interface is configured to perform time division multiplexing using the channels between the processor nodes.

11. (currently amended) The system of claim 9 wherein at least one of the first communication interface and the second ~~the~~ communication interface is configured to perform spatial division multiplexing using the channels between the processor nodes.

12. (currently amended) The system of claim 1 wherein at least one of the first communication interface and the second ~~the~~ communication interface comprises a processor network interface.

13. (currently amended) The system of claim 1 wherein at least one of the first communication interface and the second ~~the~~ communication interface comprises a processor network switch.

14. (currently amended) The system of claim 1 wherein at least one of the first communication interface and the second ~~the~~ communication interface comprises a standard input/output interface.

15. (canceled)

16. (currently amended) The system of claim 1 wherein at least one of the first communication interface and the second ~~the~~ communication interface comprises a multiplexer/demultiplexer.

17. (canceled)

18. (currently amended) A method for a system with multiple processor nodes, the method comprising:

executing an application in at least one processing element in a plurality of the processor nodes;

providing an additional new instruction to a set of standard instructions for the processing element, using at least one software extensible device in the plurality of the processor nodes, wherein the new instructions can be programmed by software; ~~and~~

communicating using a first communication interface including a first array interface module configured to interface to a first other member of the plurality of processing nodes;

determining if a neighboring device is a member of the plurality of processor nodes;

if the neighboring device is a member of the plurality of processing nodes, communicating to the neighboring device using a second communication interface including a second array interface module; and

if the neighboring device is not a member of the plurality of processing nodes, communicating to the neighboring device using a standard input/output interface of the second communication interface.

~~communicating between the processor nodes using at least one communication interface in a plurality of the processor nodes using different communication protocols based on whether or not a neighboring processor node comprises another software extensible device and whether the neighboring processor node is on a separate chip or on a same chip.~~

19. (canceled)

20. (currently amended) The method of claim 18 wherein communicating using a first communication interface including a first array interface module ~~communicating between the processor nodes~~ comprises using message passing.

21. (currently amended) The method of claim 18 wherein communicating using a first communication interface including a first array interface module ~~communicating between the processor nodes~~ comprises using channels between the processor nodes.

22. (original) The method of claim 21 wherein using the channels between the processor nodes further comprises performing time division multiplexing with the channels.

23. (original) The method of claim 21 wherein using the channels between the processor nodes further comprises performing spatial division multiplexing with the channels.

24. (original) The method of claim 18 further comprising compiling the application.

25. (original) The method of claim 18 further comprising loading the application into one of the plurality of the processor nodes.

26. (currently amended) The method of claim 18 further comprising configuring one of the processor nodes to select between an array interface module and a standard input/output interface based on a type of the ~~on a~~ neighboring device.

27. (canceled)

28. (canceled)

29. (canceled)

30. (canceled)

31. (new) The system of claim 1 wherein each processor node further comprises:

a third communication interface including a third array interface module configured to interface to a third other member of the plurality of processor nodes, and a third standard input/output interface configured to communicate with a third input/output device, and

a fourth communication interface including a fourth array interface module configured to interface to a fourth other member of the plurality of processor nodes, and a fourth standard input/output interface configured to communicate with a fourth input/output device.

32. (new) The system of claim 1 wherein the first communication interface is configured to communicate through the first array interface module if the first communication interface is coupled to the first other member of the plurality of processing nodes, and to communicate through the first standard input/output interface if the first communication interface is coupled to the first input/output device.

33. (new) The system of claim 1 wherein two or more of the plurality of processor nodes are configured in a one-dimensional array.

34. (new) The system of claim 1 wherein three or more of the plurality of the processor nodes are configured in a non-rectangular configuration.

35. (new) The system of claim 10 wherein the time division multiplexing provides a guaranteed bandwidth for a communication between the processing nodes.

36. (new) The system of claim 1 wherein the first communication interface is configured to guarantee a bandwidth for a communication between two of the plurality of processor nodes.

37. (new) The method of claim 18 further comprising:

determining if another neighboring device is a member of the plurality of processor nodes;

if the another neighboring device is a member of the plurality of processing nodes, communicating to the another neighboring device using a third communication interface including a third array interface module; and

if the another neighboring device is not a member of the plurality of processing nodes, communicating to the neighboring device using a standard input/output interface of the third communication interface.

38. (new) The method of claim 18 wherein the communicating using the first communication interface uses the first array interface module and uses time division

multiplexing, the time division multiplexing providing a guaranteed bandwidth for a communication to the first other member of the plurality of processor nodes.